Practical Training for Nanotech Master – 2004/2005

C3: Characterization of Submicronic MOS Transistors
- Short Channel Effects and Parameters Extraction -

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Introduction

The devices tested in this practical training of 4 hours come from wafers processed with a *STMicroelectronics* bulk technology. The oxide gate is an RNT oxide with a thickness as small as 12 Å, leading to a significant level of tunnel current investigated here. The smaller physical gate length is *around* 35 nm.

The aims of this practical training are:

1°) overview of basic parameters extraction methodologies using static characteristic of MOS transistors,
2°) experimental evidences of advanced physical effects such as Tunnelling current and its impact of drain current measurements, mobility degradation due to surface roughness, V_T roll off and Drain Induce Barrier Lowering.

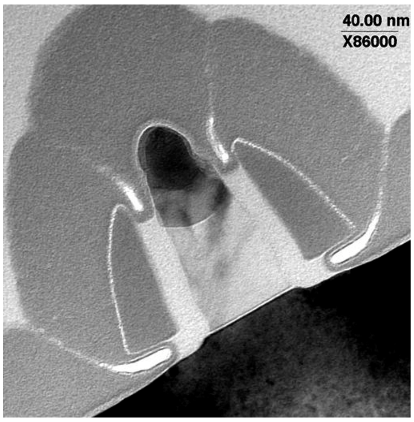
The different characteristics of the transistors are the followings:

- NMOS Transistor
- gate oxide : nitride SiO_2 (by RNT), thickness 12 Å
- Si-poly gate, thickness 150 nm
- LDD extension with As for NMOS and B for PMOS
- pockets implants with B for NMOS and Ph for PMOS
- source and drain siliced $CoSi_2$.
- battery transistors with common source and gate

W = 10 µm,

L = 10 ; 5 ; 1 ; 0.465 ; 0.285 ; 0.185 ; 0.145 ; 0.125 ; 0.105 ; 0.085 ; 0.055 ; 0.035 µm.

- isolated transistors W = 10 µm, L = 10 µm ; 0.285 µm ; 0.150 ; 0.055 and 0.035 µm.



TEM picture of the MOSFET (STMicroelectronics)

0 Recall :

In the linear region, drain current as function of gate voltage is given by: $I_d(V_g, V_d) = \frac{W}{L}\mu_{eff}(V_g)\, Q_i(V_g)\, V_d$, where:

- $Q_i(V_g) \approx C_{ox}\,(V_g - V_T - \frac{V_d}{2})$ represents the inversion charge in strong inversion[1] .

- $\mu_{eff}(V_g) = \dfrac{\mu_0}{1 + \theta_1\,(V_g - V_T - \frac{Vd}{2}) + \theta_2\,(V_g - V_T - \frac{Vd}{2})^2}$ is the effective mobility in strong inversion.

Definition of the different parameters:

θ_1 and θ_2 are the linear and quadratic mobility attenuation coefficients respectively, both due to surface roughness scattering.
$g_m(V_g) = \dfrac{\partial I_d}{\partial V_g}$ is the ohmic transconductance, $\beta_0 = \frac{W}{L} C_{ox}\,\mu_0$, The Y function is given by : $Y(V_g) = \dfrac{I_d(V_g)}{\sqrt{g_m(V_g)}}$

✍01 Give the units of the different parameters above.

✍02 Recall what are SCE and DIBL (definition + you can help yourself with a drawing…).

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[1] The term $V_d/2$ (not seen during the lecture) is only necessary when V_d is not negligible (V_d > 10 mV)

I Measurements – observation of the DIBL:

Measurements on battery transistors

✍11 Preliminary measurements:
Measure and plot $I_d(V_d)$ curves for a long channel (5µm for example) for V_g=0 to 1V with V_d from 0 to 1V (step 40mV). Comment (different regions, linear regime, saturation regime…).

✍12 Calculate the saturation speed υ_{sat} (I_{dsat} will be determined for V_d=1V).
Recall: $I_{dsat}=W\ C_{ox}\ \upsilon_{sat}(V_g-V_t)$

✍13 Measure and plot $I_d(V_d)$ curves at V_g=1V for the different gate lengths of the battery transistors (V_d: 0 to 1V, step 40 mV). Comment (impact of gate length reduction on the characteristics …).
Plot $Id_{sat\ short\ channel}$ / $Id_{sat\ long\ channel}$ (10µm) as function of the ratio Lg_{long}/Lg_{short}. Comment. Why is not linear?

✍14 Compare the $I_d(V_d)$ curves for a long channel (5µm for example) and a short channel (0.1µm and less) in the two following cases : V_g above and under the threshold (1V and 0.1 for example). Explain the differences.

✍15 Determine the threshold voltage for the different gate lengths in the linear region. You can use in a first time the Vt value taken from the normalised Id, 10^{-7}.W/L (A). How can you easily measure ΔV_T as a function of L (in weak inversion)? Are the different values consistent? (this analysis will be carried out further with the accurate Vt values extracted from the improved Y function method for example).

✍16 Measure and plot $I_d(V_g)$ curves (logarithmic scale) for different Vd (0 to 1V step 100mV) and for different gate lengths (long to short channel), Vg from 0 to 1V step 40mV. Comment. Which effect is observed? Explain it.

✍17 Plot DIBL curve (you can measure some others gate lengths in the linear region, V_d=10mV for example, and the saturated region, V_d=1V).
Plot also I_{OFF} and I_{ON} versus L_g.
Finally plot $I_{OFF}(I_{ON})$.
Recall : $I_{OFF}=I_d$ at V_g=0V and V_d=1V. $I_{ON}=I_d$ at $V_g=V_d$=1V.
Comment. Up to which Lg the technology is interesting in term of ratio performance/consumption? Which are the main limiting phenomena?

II Impact of the ultrathin oxide on the drain current in the linear region:

Measurements on isolated transistors

✍21 Measure I_d as function as V_g (0 to 1V step 20mV) in the linear region for V_d = 10 mV and for the different gate length of the isolated transistors. Record also I_s et I_g.

✍22 Plot I_d, I_g, I_s(Vg) (on the same graph) and I_d and g_m(Vg). Comment.
Propose a method to correct the drain current of the gate leakage (drain current if the gate leakages were negligible, I_{D0} or I_{ch} for channel current) in the linear region.
The gate current will be divided into two part; the first which represents the gate current near the source and the second near the drain (partition coefficients α_S and α_D respectively, $I_{gtotal}=\alpha_S.I_g+\alpha_D.I_g$).
Make a drawing of the MOS structure with the different currents.

✍23 It is also possible to correct the drain current in the case of battery transistors. In that case, we use the relation $I_d=g_d.V_d$ where g_d is the conductance determined from two measurements at low V_d.
Try this method on both isolated and battery transistors with long and short channels.

III Parameters Extraction in the linear region from static characteristics

✍30 Preliminary question: Why is it interesting to extract the parameters in the linear region?

✍31 Preliminary measurements:
Calculate and plot g_m and Id for different Vg steps (for example 10 mV and 50 mV) and for different integration time (long and short). Conclusion (impact of the measurement conditions, interpretation of noise influence…)?

III-1 The θ_2 parameter for submicronic MOSFETs:

If θ_2=0 (Classical MOSFET, studied in the practical work C2), Y function in strong inversion region is given by:

$$Y(V_g)=\sqrt{G_mV_d}\,(V_g-V_T-\frac{V_d}{2})$$

Y is thus a linear function of V_g, allowing a possible extraction of the threshold voltage V_T and the G_m parameter.

✍311 How can we define experimentally the strong inversion regime?

✍312 Observe $Y(V_g)$ for all devices. Conclusion and interpretations?
When $\theta_2\neq0$, simple calculation show that the real expression of the Y function is given by:

$$Y(V_g)=\sqrt{\frac{G_mV_d}{1-\theta_2(V_g-V_T-\frac{V_d}{2})^2}}\,(V_g-V_T-\frac{V_d}{2})=\frac{Y_{\theta_2=0}(V_g)}{\sqrt{1-\theta_2(V_g-V_T-\frac{V_d}{2})^2}} \qquad (1)$$

Explain why this formula is consistent with yours observations. To overcome this problem, we propose three new extraction techniques: the improved Y function method, the Hamer method and the inverse drain current second derivative method.

III-2 Improved Y function method:

It's an extension of the former Y function approach. It consists in:

- First, extracting the V_{T0} and G_{m0} approximated values of the real V_T and G_m.
- Secondly, calculating the θ_{eff} parameter given by the following formula :

$$\theta_{eff} = \frac{G_{m0} V_d}{I_d} - \frac{1}{V_g - V_{T0} - \frac{V_d}{2}}$$

If V_{T0} et G_{m0} were accurate, θ_{eff} would be equal to $\theta_1 + \theta_2 (V_g - V_T - V_d/2)$. As V_{T0} et G_{m0} values are only approximated value of the real V_T and G_m, the values θ_{10} and θ_{20} obtained by such an extraction will be also approximated values of the real θ_1 and θ_2. The next step consists in trying to calculate a new Y function, with no more non linearity due to θ_2. To this aim, we calculate a second Y function, Y_0, defined as:

$$Y_0 = Y_{meas} \times \sqrt{1 - \theta_{20} \left(V_g - V_{T0} - \frac{V_d}{2} \right)^2}$$

If θ_{20} is equal to the accurate value of θ_2, according to Eq. (1), we should have $Y_0 = \sqrt{G_m V_d}\,(V_g - V_T - \frac{Vd}{2})$.

Generally, this is not exactly the case, but Y_0 function exhibits a more linear dependency versus V_g than the measured Y function. New V_T, G_m, θ_1 and θ_2 parameters can then be extracted from Y_0, following the same procedure until convergence (good linearity of Y_n function as function of V_g requires usually 2 or 3 iterations).

Finally, after these two or three steps, the values of V_{Ti}, G_{mi}, θ_{1i} and θ_{2i} (i = 1 or 2) are closed to the real values of V_T, G_m, θ_1, and θ_2.

✍321 Clarify by the calculation the different stages of this procedure (see article [MOURRAIN 00] for help).

✍322 Apply this method for one transistor.

III-3 Hamer Method:

It's an optimisation procedure based on a numerical fitting algorithm (Levenberg Macquardt). Details of this algorithm will not be investigated here. It consists in searching the G_m, V_T, θ_1 et θ_2 parameters which will best fit the experimental data points according the relation:

$$I_d(V_g, V_d) = \frac{G_m V_d\,(V_g - V_T - \frac{V_d}{2})}{1 + \theta_1\,(V_g - V_T - \frac{V_d}{2}) + \theta_2\,(V_g - V_T - \frac{V_d}{2})^2}$$

✍3331 Apply this method for the same transistor previously tested.

III-4 Inverse drain current second derivative method:

✍341 Calculate $1/I_d$ in the linear region.

✍342 Calculate $d(1/I_d)/dV_g$.

✍343 Calculate then $d^2(1/I_d)/dV_g^2$. Which parameters can you extract? (explain which plot will have to be done… see article [McLARTY 95] for help)

✍344 Compare these results to those obtained with the improved Y method.

✍345 What are the advantages and the drawbacks of these three extraction methods?

✍346 Determine the parameters of all the transistors.

III-5 Series resistance Extraction:

✍351 If the series resistances (R_{SD}) are not negligible, the drain current will be affected. The G_m, V_T, θ_1 and θ_2 parameters can thus be modified. Demonstrate by calculation that only θ_1 is affected (give moreover a diagram of the transistor with its R_{SD} and the different voltages).

✍352 Give a solution to extract the R_{SD} and the true value of θ_1, θ_1^*. Extract then R_{SD} and θ_1^*. (Assuming that $R_S = R_D = R_{SD}/2$)

III-6 Effective Gate Length Extraction:

✍361 In reality, the true value of the channel length (L_{eff}) is not exactly equal to the nominal value (called sometimes mask length L_m). Assuming $\Delta L = L_m - L_{eff}$ is a constant parameter, how can we extract ΔL?

✍362 Deduce from yours measurements the values of ΔL and μ_0, the low field mobility.